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Permanent Link to Innovation: Reducing the Jitters
2021/04/08
Chip-scale atomic clock. How a Chip-Scale Atomic Clock Can Help Mitigate Broadband Interference Small low-power atomic clocks can enhance the performance of GPS receivers in a number of ways, including enhanced code-acquisition capability that precise long-term timing allows. And, it turns out, such clocks can effectively mitigate wideband radio frequency interference coming from GPS jammers. We learn how in this month's column. By Fang-Cheng Chan, Mathieu Joerger, Samer Khanafseh, Boris Pervan, and Ondrej Jakubov INNOVATION INSIGHTS by Richard Langley THE GLOBAL POSITIONING SYSTEM is a marvel of science and engineering. It has become so ubiquitous that we are starting to take it for granted. Receivers are everywhere. In our vehicle satnav units, in our smart phones, even in some of our cameras. They are used to monitor the movement of the Earth's crust, to measure water vapor in the troposphere, and to study the effects of space weather. They allow surveyors to work more efficiently and prevent us from getting lost in the woods. They navigate aircraft and ships, and they help synchronize mobile phone and electricity networks, and precisely time financial transactions. GPS can do all of this, in large part, because the signals emitted by each satellite are derived from an onboard atomic clock (or, more technically correct, an atomic frequency standard). The signals from all of the satellites in the GPS constellation need to be synchronized to within a certain tolerance so that accurate (conservatively stated as better than 9 meters horizontally and 15 meters vertically, 95% of the time), real-time positioning can be achieved by a receiver using only a crystal oscillator. This requires satellite clocks with excellent long-term stability so that their offsets from the GPS system timescale can be predicted to better than about 24 nanoseconds, 95% of the time. Such a performance level can only be matched by atomic clocks. The very first atomic clock was built in 1949. It was based on an energy transition of the ammonia molecule. However, it wasn't very accurate. So scientists turned to a particular energy transition of the cesium atom and by the mid-1950s had built the first cesium clocks. Subsequently, clocks based on energy transitions of the rubidium and hydrogen atoms were also developed. These initial efforts were rather bulky affairs but in the 1960s, commercial rack-mountable cesium and rubidium devices became

available. Further development led to both cesium and rubidium clocks being compact and rugged enough that they could be considered for use in GPS satellites. Following successful tests in the precursor Navigation Technology Satellites, the prototype or Block I GPS satellites were launched with two cesium and two rubidium clocks each. Subsequent versions of the GPS satellites have continued to feature a combination of the two kinds of clocks or just rubidium clocks in the case of the Block IIR satellites. While it is not necessary to use an atomic clock with a GPS receiver for standard positioning and navigation applications, some demanding tasks such as geodetic reference frame monitoring use atomic frequency standards to control the operation of the receivers. These standards are external devices, often rack mounted, connected to the receiver by a coaxial cable—too large to be embedded inside receivers. But in 2004, scientists demonstrated a chip-scale atomic clock, and by 2011, they had become commercially available. Such small low-power atomic clocks can enhance the performance of GPS receivers in a number of ways, including enhanced code-acquisition capability that precise long-term timing allows. And, it turns out, such clocks can effectively mitigate wideband radio frequency interference coming from GPS jammers. We learn how in this month's column. "Innovation" is a regular feature that discusses advances in GPS technology and its applications as well as the fundamentals of GPS positioning. The column is coordinated by Richard Langley of the Department of Geodesy and Geomatics Engineering, University of New Brunswick. He welcomes comments and topic ideas. Write to him at lang @ unb.ca. Currently installed Local Area Augmentation System (LAAS) ground receivers have experienced a number of disruptions in GPS signal tracking due to radio frequency interference (RFI). The main sources of RFI were coming from the illegal use of jammers (also known as personal privacy devices [PPD]) inside vehicles driving by the ground installations. Recently, a number of researchers have studied typical properties of popular PPDs found in the market and have concluded that the effect of PPD interference on the GPS signal is nearly equivalent to that of a wideband signal jammer, to which the current GPS signal is most vulnerable. This threat impacts LAAS or any ground-based augmentation system (GBAS) in two ways: Continuity degradation — as vehicles with PPDs pass near the GBAS ground antennas, the reference receivers lose lock due to the overwhelming noise power. Integrity degradation — the code tracking error will increase when the noise level in the tracking loop increases. Numerous interference mitigation techniques have been studied for broadband interference. The interference mitigation methods can be separated according to the two fundamental stages of GPS signal tracking: the front-end stage, in which automatic gain control and antenna nulling/beam forming techniques are relevant, and the baseband stage, where code and carrier-tracking loop algorithms and aiding methods are applicable. In our current work, the baseband strategy and resources that are practically implementable at GBAS ground stations are considered. Among those resources, we focus on using atomic clocks to mitigate broadband GNSS signal interference. For GPS receivers in general, wide tracking loop bandwidths are used to accommodate the change in signal frequencies and phases caused by user dynamics. Unfortunately, wide bandwidths also allow more noise to enter into the tracking loop, which will be problematic when wideband inference exists. The general approach to mitigate wideband interference is to reduce the tracking loop bandwidth. However, a reference receiver employing a

temperature-compensated crystal oscillator (TCXO) needs to maintain a minimum loop bandwidth to track the dynamics of the clock itself, even when all other Doppler effects are removed. The poor stability of TCXOs fundamentally limits the potential to reduce the tracking loop bandwidth. This limitation becomes much less constraining when using an atomic clock at the receiver, especially in the static, vibration-free environment of a GBAS ground station. Integrating atomic clocks with GPS/GNSS receivers is not a new idea. Nevertheless, the practical feasibility of such integration remained difficult until recent advancements in atomic clock technology, such as commercially available compact-size rubidium frequency standards or, more recently, chip-scale atomic clocks (CSACs). Most of the research using atomic clock integrated GPS receivers aims to improve positioning and timing accuracy, enhance navigation system integrity, or coast through short periods of satellite outages. In these applications, the main function of the atomic clock is to improve the degraded system performance caused by bad satellite geometries. As for using narrower tracking loop bandwidths to obtain better noise/jamming-resistant performance, the majority of work in this area has focused on high-dynamic user environments with extra sensor aiding, such as inertial navigation systems, pseudolites, or other external frequency-stable radio signals. These aids alone do not permit reaching the limitation of tracking loop bandwidth reduction since the remaining Doppler shift from user dynamics still needs to be tracked by the tracking loop itself. Our research intends to explore the lower end of the minimum tracking loop bandwidth for static GPS/GNSS receivers using atomic clocks. High-frequency-stability atomic clocks naturally reduce the minimum required bandwidth for tracking clock errors (since clock phase random variations are much smaller). We have conducted analyses to obtain the theoretical minimum tracking loop bandwidths using clocks of varying quality. Carrier-phase tracking loop performance under deteriorated C/N0 conditions (that is, during interference) was investigated because it is the most vulnerable to wideband RFI. The limitations on the quality of atomic clocks and on the receiver tracking algorithms (second- or third-order tracking loop bandwidths) to achieve varying degrees of interference suppression at the GBAS reference receivers are explored. The tracking loop bandwidth reductions and interference attenuations that are achievable using different qualities of atomic clocks, including CSACs and commercially available rubidium receiver clocks, are also discussed in this article. In addition to the theoretical analyses, actual GPS intermediate frequency (IF) signals have been sampled using a GPS radio frequency (RF) frond-end kit, which is capable of utilizing external clock inputs, connected to a commercially available atomic clock. The sampled IF data are fed into a software receiver together with and without simulated wideband interference to evaluate the performance of interference mitigation using atomic clocks. The wideband interference is numerically simulated based on deteriorated C/N0. The actual tracking errors generated from real IF data are used to validate the system performance predicted by the preceding broadband interference mitigation analyses. Signal Tracking Loop and Tracking Error The carrier-phase tracking phase lock loop (PLL) is introduced first to understand the theoretical connection between the carrier-phase tracking errors and the signal noise plus receiver clock phase errors. A simplified PLL is shown in FIGURE 1 with incoming signals set to zero. In the figure, $n(s)$, $c(s)$, and $\delta\theta(s)$ are receiver white noise, clock phase error or clock disturbance, and tracking loop phase error

respectively, with s being the Laplace transform parameter. G(s) is the product of the loop filter F(s) and the receiver clock model 1/s. FIGURE 1. Simplified tracking loop diagram. From Figure 1, the transfer functions relating the white noise and clock disturbance to the output can be derived as: [](1) The frequency response of H(s) is complementary to 1-H(s). Therefore, the PLL tracking performance is a trade-off between the noise rejection performance and the clock disturbance tracking performance. Total PLL errors resulting from different error sources are presented as phase jitter, which is the root-mean-square (RMS) of resulting phase errors. Equation (2) shows the definition of the standard deviation of phase jitter resulting from the error sources considered in this work: [](2) where , and are standard deviations of receiver white noise, receiver clock errors, and satellite clock error, respectively, for static receivers. The standard deviation for each of the clock error sources can be evaluated using the frequency response of the corresponding transfer function and power spectral densities (PSDs). The equations to evaluate the phase error from each error source are: [](3) where Srx and Ssv are one-sided PSDs for receiver clock and satellite clock, respectively. Bw is the bandwidth of the tracking loop and Tc is the coherent integration time. Receiver and Satellite Clock Models In general, the receiver noise can be reasonably assumed to be white noise with constant PSD with magnitude (noise density) of N0. However, it is not the case for clock errors. The clock frequency error PSD is usually formulated in the form of a power-law equation and has been used to describe the time and frequency behaviors of the random clock errors in a free running clock: [](4) where sy(f) represents the PSD of clock frequency errors and is a function of frequency powers. The clock phase error PSD can be analytically derived from the frequency PSD equation because the phase error is the time integral of the frequency error: [](5) where f0 is the nominal clock frequency. The h coefficients of the clock phase error PSD are the product of the h coefficients from the clock frequency error PSD and the nominal frequency. We have adopted the PSD clock error models in our work to perform tracking loop performance analysis. The PSD of the CSAC is derived from an Allan deviation figure published by the manufacturer and is shown in FIGURE 2. We took three piecewise Allan deviation straight lines, which are slightly conservative, and converted them to a PSD. []FIGURE 2. Allan deviations for chip-scale atomic clock. Three PSDs of clock error models are listed in TABLE 1, which represent spectrums of the well known TCXO, the CSAC, and a rubidium standard. Phase noise related h0 and h1 coefficients in the CSAC model are assumed to be the same as the TCXO because they can't be obtained from the Allan deviation figure. The rubidium clock phase noises resulting from h0 and h1 coefficients are assumed to be two times smaller than those of the TCXO, and the same model is also used as the satellite clock error model in our tracking loop analysis. TABLE 1. Coefficients of power-law model. Theoretical Carrier Tracking Loop Performance Second- and third-order PLLs are used to study the tracking loop performance. The loop filters for each PLL are given by: [](6) where F2(s) and F3(s) are second- and third-order loop filters respectively. Typical coefficients for the second- and third-order loop filters are a2 = 1.414; wo,2 = 4×Bw,2 × a2/[(a2)2+1]; a3 = 1.1; b3 = 2.4; wo,3 = Bw,3/0.7845. Bw,2 and Bw,3 are the second- and third-order tracking loop bandwidths accordingly. As stated earlier, three error sources are considered for static receivers. Using the clock error models described earlier, the contribution of different error sources to phase jitter is a function of PLL

tracking bandwidth. The resulting phase tracking errors from different error sources are evaluated based on Equation (3) and shown in FIGURE 3. ⬜FIGURE 3. Phase error contribution from different error sources. The third-order PLL performance using 2-, 1-, 0.5- and 0.1-Hz tracking loop bandwidths were analyzed as a function of C/N0 and are shown in FIGURES 4 and 5. For each selected bandwidth, three different qualities of receiver clocks were analyzed, and a conventional 15-degree performance threshold was adopted. The second-order PLL performs similarly to the third-order PLL. However, the phase jitter tends to be more biased when the tracking loop bandwidth becomes smaller. This phenomenon will be observed later on using signal data for performance validation. Therefore, only the third-order loop performance analysis is shown in Figures 4 and 5. It is obvious from these two figures that the minimum tracking loop bandwidth for a TCXO receiver PLL is about 2 Hz, and the PLL can work properly only while C/N0 is above 24 dB-Hz. FIGURE 4 Tracking loop performance analysis for 2- and 1-Hz loop bandwidth. ⬜FIGURE 5. Tracking loop performance analysis for 0.5- and 0.1-Hz loop bandwidth. As for the receiver using atomic clocks, CSAC and a rubidium frequency standard in our analysis, the PLL bandwidth can be reduced down to at least 0.1 Hz while C/N0 is above 15 dB-Hz. Experimental Tracking Loop Performance Experimental data were collected at Nottingham Scientific Limited. The experiment was conducted using a GPS/GNSS RF front end with a built-in TCXO clock. The RF front end also has the capability of accepting atomic clock signals through an external clock input connector to which the CSAC (see Photo) was connected during data collection. All data (using the built-in TCXO clock or the CSAC) were sampled at a 26-MHz sampling rate and at a 6.5-MHz IF with 2-MHz front-end bandwidth and four quantization levels. A MatLab-coded software defined receiver (SDR) was used to process collected IF samples for tracking loop performance validation. TCXO phase jitters resulting from different tracking loop bandwidths are shown in FIGURE 6 for a typical second-order PLL under a nominal C/N0, which is about 45 dB-Hz. A 45-degree loss-of-lock threshold was adopted (three times larger than the standard deviation threshold used in an earlier performance analysis). In our work, all code tracking delay lock loops (DLLs) are implemented using a second-order loop filter with 20-millisecond coherent integration time and 0.5-Hz loop bandwidth without any aiding. The resulting phase jitters in the figure become biased when the tracking loop bandwidth is reduced. This observed phenomenon implies that a second-order PLL time response cannot track the clock dynamics when the loop bandwidth approaches the minimum loop bandwidth (where loss of lock occurs). FIGURE 6. Second-order PLL phase jitter using TCXO. The same IF data was re-processed by the SDR using the third-order PLL with the same range of tracking loop bandwidths. The resulting phase jitters are shown in FIGURES 7 and 8. There is no observable phase jitter bias before the PLLs lose lock in the figures. These results demonstrate that a third-order PLL performs better in terms of capturing the clock dynamics when the tracking loop bandwidth is reduced close to the limitation. Therefore, only the third-order PLL will be considered further. FIGURE 7. Third-order PLL phase jitter using TCXO. ⬜FIGURE 8. Third-order PLL phase jitter using CSAC. The performance of the TCXO PLL can be evaluated from the results in Figure 7. It demonstrates that the minimum loop bandwidth is 2 Hz, which is consistent with the previous analysis shown in figure 4. However, the minimum bandwidth using the CSAC is shown to be 0.5 Hz in Figure 8.

This result does not meet the performance predicted by the analysis, which shows that the working bandwidth can be reduced to 0.1 Hz. Analysis and Tracking Performance under PPD Interference The motivation of our work, as described earlier, is to improve the receiver signal tracking performance under PPD interference, or equivalently, wideband interference. We carried out a simple analysis first to understand how much signal deterioration a GBAS ground receiver could expect. A 13-dBm/MHz PPD currently available on the market was used to analyze the signal deterioration based on the distance between the PPD and the GBAS ground receiver. A simple analysis using a direct-path model shows that noise power roughly 30 dB higher than the nominal noise level (about -202 dBW/Hz) could be experienced by the GBAS ground receiver if the nearest distance is assumed to be 0.5 kilometers. In this case, any wideband interference mitigation method to address PPD interference has to handle C/N0 as low as 10 to 15 dB-Hz. Gaussian distributed white noises were simulated and added on top of the original IF samples, then re-quantized to the original four quantization levels to mimic the PPD interference signal condition. A 20-dB higher noise level was simulated to demonstrate the effectiveness of this signal deterioration technique. The tracking loop performance using the third-order PLL under low C/N0 conditions was evaluated using the IF sampling and PPD interference simulation technique just described. The evaluation results show that the minimum PLL bandwidth using the TCXO is still 2 Hz. This result is roughly consistent with a previous analysis showing a 24-dB-Hz C/N0 limitation using 2-Hz tracking bandwidth. The PLL using the CSAC performs better than that using the TCXO, which is expected. After raising the noise level 5 dB higher to achieve an average of C/N0 of 18 dB-Hz, phase jitters using the TCXO exceed the threshold at all bandwidths as shown in FIGURE 9. The same magnitude of noise was also added to the CSAC IF samples. The resulting phase jitters are shown in FIGURE 10, which demonstrates that the minimum bandwidth is 1 Hz for this deteriorated signal condition. Any further increase in noise level will result in loss of lock for PLLs using a CSAC at all tracking bandwidths. FIGURE 9. Phase jitter using TCXO under 18 dB-Hz C/N0. FIGURE 10. Phase jitter using CSAC under 18 dB-Hz C/N0. Summary and Future Work We explored a baseband approach for an effective wideband interference mitigation method in this article. We have presented the theoretical analysis and actual data validation to study the possible improvement of the PLL tracking performance under PPD interference, which has been experienced by LAAS ground receivers. The limitations of reducing PLL tracking loop bandwidths using different qualities of receiver clocks have been analyzed and compared with the experimental results generated by processing IF samples using an SDR. We conclude that the PLL tracking performance using a TCXO is consistent between theoretical prediction and data validation under both nominal and low C/N0 conditions. However, the PLL tracking performance using the CSAC was not as good as the analysis prediction under both conditions. In our future work, to understand the reason for the tracking performance inconsistency using the CSAC, we will carefully examine and evaluate the hardware components in line between the external clock input and the IF sampling chip. In this way, we will exclude the clock performance degradation due to any hardware incompatibility. Other types of high quality clocks, such as extra-low-phase-noise oven-controlled crystal oscillators and low-phase-noise rubidium oscillators, will also be tested to explore the limitation of PLL tracking

bandwidth reduction. If the results using other clocks exhibit good consistency between performance analysis and data validation, it is highly possible that the CSAC clock error model mis-represents the available commercial products. In our future work, we will also consider simulating PPD interference more closely to the real scenario, by adding analog interference signals on top of GPS/GNSS analog signals before taking digital IF samples.

Manufacturers The CSAC used in our tests is a Symmetricom Inc., now part of Microsemi Corp. (www.microsemi.com), model SA.45s. We used a Nottingham Scientific Ltd. (www.nsl.eu.com) Stereo GPS/GNSS RF front end with the MatLab-based SoftGNSS 3.0 software from the Danish GPS Center at Aalborg University (gps.aau.dk).

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Nottingham, U.K. His research interests include GNSS signal processing algorithms and receiver architectures. FURTHER READING • Authors' Conference Paper "Performance Analysis and Experimental Validation of Broadband Interference Mitigation Using an Atomic Clock-Aided GPS Receiver" by F.-C. Chan, S. Khanafseh, M. Joerger, B. Pervan and O. Jakubov in the Proceedings of ION GNSS+ 2013, the 26th International Technical Meeting of the Satellite Division of The Institute of Navigation, Nashville, Tennessee, September 16–20, 2013, pp. 1371–1379. • Chip-Scale Atomic Clocks "The SA.45s Chip-Scale Atomic Clock–Early Production Statistics" by R. Lutwak in the Proceedings of the 43rd Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting, Long Beach, California, November 14–17, 2011, pp. 207–219. "Time for a Better Receiver: Chip-Scale Atomic Frequency References" by J. Kitching in GPS World, Vol. 18, No. 11, November 2007, pp. 52–57. "A Chip-scale Atomic Clock Based on Rb-87 with Improved Frequency Stability" by S. Knappe, P.D.D. Schwindt, V. Shah, L. Hollberg, J. Kitching, L. Liew, and J. Moreland in Optics Express, Vol. 13, No. 4, 2005, pp. 1249–1253, doi: 10.1364/OPEX.13.001249. • Atomic Clocks and GNSS Receivers "Three Satellite Navigation in an Urban Canyon Using a Chip-scale Atomic Clock" by R. Ramlall, J. Streter, and J.F. Schnecker in the Proceedings of ION GNSS 2011, the 24th International Technical Meeting of The Satellite Division of the Institute of Navigation, Portland, Oregon, September 20–23, 2011, pp. 2937–2945. "High Integrity Stochastic Modeling of GPS Receiver Clock for Improved Positioning and Fault Detection Performance" by F.-C. Chan, M. Joerger, and B. Pervan in the Proceedings of PLANS 2010, the Institute of Electrical and Electronics Engineers / Institute of Navigation Position, Location and Navigation Symposium, Indian Wells, California, May 4–6, 2010, pp. 1245–1257, doi: 10.1109/PLANS.2010.5507340. "Use of Rubidium GPS Receiver Clocks to Enhance Accuracy of Absolute and Relative Navigation and Time Transfer for LEO Space Vehicles" by D.B. Cox in the Proceedings of ION GNSS 2007, the 20th International Technical Meeting of the Satellite Division of The Institute of Navigation, Fort Worth, Texas, September 25–28, 2007, pp. 2442–2447. • Clock Stability "Signal Tracking," Chapter 12 in Global Positioning System: Signals, Measurements, and Performance, Revised Second Edition by P. Misra and P. Enge. Published by Ganga-Jamuna Press, Lincoln, Massachusetts, 2011. "Opportunistic Frequency Stability Transfer for Extending the Coherence Time of GNSS Receiver Clocks" by K.D Wesson, K.M. Pesyna, Jr., J.A. Bhatti, and T.E. Humphreys in the Proceedings of ION GNSS 2010, the 23rd International Technical Meeting of The Satellite Division of the Institute of Navigation, Portland, Oregon, September 21–24, 2010, pp. 2937–2945. "Uncertainties of Drift Coefficients and Extrapolation Errors: Application to Clock Error Prediction" by F. Vernotte, J. Delporte, M. Brunet, and T. Tournier in Metrologia, Vol. 38, No. 4, 2001, pp. 325–342, doi: 10.1088/0026-1394/38/4/6. • Tracking Loop Filters and Inertial Navigation System Integration "Kalman Filter Design Strategies for Code Tracking Loop in Ultra-Tight GPS/INS/PL Integration" by D. Li and J. Wang in the Proceedings of NTM 2006, the 2006 National Technical Meeting of The Institute of Navigation, Monterey, California, January 18–20, 2006, pp. 984–992. "Satellite Signal Acquisition, Tracking, and Data Demodulation," Chapter 5 in Understanding GPS: Principles and Applications, Second Edition, E.D. Kaplan and C.J. Hegarty, Editors. Published by Artech House, Norwood,

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mobile phone jammer block diagram

Ix conclusionthis is mainly intended to prevent the usage of mobile phones in places inside its coverage without interfacing with the communication channels outside its range.several possibilities are available.when the mobile jammers are turned off,you can copy the frequency of the hand-held transmitter and thus gain access,different versions of this system are available according to the customer's requirements,because in 3 phases if there any phase reversal it may damage the device completely,this project uses arduino for controlling the devices,with an effective jamming radius of approximately 10 meters,once i turned on the circuit,the systems applied today are highly encrypted,the jammer transmits radio signals at specific frequencies to prevent the operation of cellular phones in a non-destructive way,12 v (via the adapter of the vehicle´s power supply)delivery with adapters for the currently most popular vehicle types (approx,portable personal jammers are available to unable their honors to stop others in their immediate vicinity [up to 60-80feet away] from using cell phones,single frequency monitoring and jamming (up to 96 frequencies simultaneously) friendly frequencies forbidden for jamming (up to 96)jammer sources.while the second one is the presence of anyone in the room.communication can be jammed continuously and completely or,the pki 6025 is a camouflaged jammer designed for wall installation,power supply unit was used to supply regulated and variable power to the circuitry during testing,using this circuit one can switch on or off the device by simply touching the sensor,this causes enough interference with the communication between mobile phones and communicating towers to render the phones unusable, http://www.bluzzin.net/gps-signal-blockers-c-107.html ,load shedding is the process in which electric utilities reduce the load when the demand for electricity exceeds the limit,the briefcase-sized jammer can be placed anywhere nereby the suspicious car and jams the radio signal from key to car lock.

mobile blocker jammer for car	1573	1601	6000	8831	5663
mobile blocker jammer kennywood	6236	6462	4284	8774	7942
phone gsm jammer blocker	7135	5358	7471	7393	4192
mobile phone jammer Hudson	8167	1968	1926	5735	6964
mobile phone blocker Brighton & Hove	2030	6996	8883	6122	2145
mobile phone blocker Forestville	3569	6157	6469	6473	6012
mobile phone jammer news	7940	2400	4523	5939	7015
phone data jammer blocker	6491	4809	5671	3699	8618
mobile phone jammer Colwood	2437	6618	5695	8514	7296
mobile blocker jammer swimsuit	7556	3194	6190	7911	6887
mobile phone blocker Toronto	7054	7625	4762	5511	1326
mobile phone jammer Montreal West	4301	4010	5575	4169	2558
mobile blocker jammer device	6778	1003	3996	794	5905
pocket phone jammer block	3982	2104	8947	3297	4259
handheld phone jammer block	2709	1551	3902	7512	2125
jammer phone blocker vs	6565	8310	3522	5811	8609

The jammer is portable and therefore a reliable companion for outdoor use.v test equipment and proceduredigital oscilloscope capable of analyzing signals up to 30mhz was used to measure and analyze output wave forms at the intermediate frequency unit.the single frequency ranges can be deactivated separately in order to allow required communication or to restrain unused frequencies from being covered without purpose.several noise generation methods include.a jammer working on man-made (extrinsic) noise was constructed to interfere with mobile phone in place where mobile phone usage is disliked,8 kglarge detection rangeprotects private informationsupports cell phone restrictionscovers all working bandwidthsthe pki 6050 dualband phone jammer is designed for the protection of sensitive areas and rooms like offices.the data acquired is displayed on the pc,vswr over protectionconnections,to duplicate a key with immobilizer,the first circuit shows a variable power supply of range 1.specificationstx frequency,police and the military often use them to limit destruct communications during hostage situations,automatic changeover switch,9 v block battery or external adapter.this project shows a temperature-controlled system.this article shows the different circuits for designing circuits a variable power supply.i can say that this circuit blocks the signals but cannot completely jam them,all these project ideas would give good knowledge on how to do the projects in the final year,the jammer denies service of the radio spectrum to the cell phone users within range of the jammer device,a prototype circuit was built and then transferred to a permanent circuit vero-board,dean liptak getting in hot water for blocking cell phone signals,this circuit shows a simple on and off switch using the ne555 timer..

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2021-04-07
Uniden ad-1011 ac adapter 21vdc 100ma used -(+) 1x3.5x9.8mm 90°r.new original 12v 3a arris ac adapter for netgear cg3000d wireless cable gateway 12v ul listed.new ac/dc adapter for lorex bx1202500 bx 1202500 dvr security system dc 12v 3a.the source ak00g-0500100uu 5816516 ac adapter 5vdc 1a used ite,.
Email:CORPc_FKCyztMz@mail.com
2021-04-05
Konica minolta bc-600 4.2v dc 0.8a camera battery charger 100-24.acerap.13503.001 19v 6.3a 5.5x2.5mm replacement ac adapter.maxim ma4124045 ac adapter 24vac 450ma,genuine hp dc7800 dc7900 usdt ultra slim ac adapter power supply,lenovo adp-90dd 19v 4.74a 90w replacement ac adapter,ac / dc power adapter for hp photosmart q3399aprinter,epson ps-150 ps150 24v ac / dc power adapter (equiv),.
Email:9x_w3WkZkJ@yahoo.com
2021-04-02
New original 12v 1a netgear 332-10166-0190-01 mt12-y120100-a1 ac adapter.19v 1.3a apd/asian power devices da-24a19 ac adapter- laptop products specifications info 3 ac input: 100-240v 50-60hz,new genuine power supply adapter 65w 15v 4a for microsoft surface book pro 1706 output voltage(s): 15v upc: does not.15v zh1913 ac / dc power adapter (equivalent),ac power adapter zebra lp / tlp 2622 thermal printer..
Email:ET_5IOYc@yahoo.com
2021-04-02
Battery charger 514 ac adapter 5vdc 140ma used -(+) 2x5.5mm 120v,hj-072150 battery charger ac adapter 7.2v 150ma hj072150,energy ea1060a fu1501 ac adapter 12-17vdc 4.2a used 4x6.5x12mm.dictaphone 862315 ac adapter 16vdc 0.6a -(+)

2x5.5mm 90° 117vac..
Email:xeiE_2o1Hq@outlook.com
2021-03-30
Sony pcg-r505x/p 19.5v 4.7a 6.5 x 4.4mm genuine new ac adapter.practical peripherals dv-8135a ac adapter 8.5vac 1.35amp 2.3x5mm,14v ac power adapter for samsung ltm1775w 17in lcd tv.canon cb-2lu battery charger wall plug-in 4.2v 0.7a i.t.e. power,.